CLAIMS

What is claimed is:

- A method comprising:
 in a processor, finding a loop in a circuit design;
 in the processor, functionally analyzing the loop; and
 - in the processor, extracting a logical element in relation to the analysis result.
- 2. The method of claim 1, comprising performing a Depth First Search linear traversal.
- 3. The method of claim 1, comprising identifying a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.
- 4. The method of claim 3, comprising generating overall zero-delay collapsed functionality on an output of said group.
- 5. The method of claim 3, comprising identifying a functional part that forms said group.
- 6. The method of claim 3, comprising determining a driving logic of said group.
- 7. The method of claim 3, comprising determining a driving control of said group.
- 8. The method of claim 3, comprising determining a stage feedback logic of said group.
- 9. The method of claim 3, comprising determining a stage feedback control of said group.
- 10. The method of claim 3, comprising determining a stage feedback type of said group.

- 11. The method of claim 3, comprising determining an asynchronous set and reset logics of said group.
- 12. The method of claim 1, comprising extracting a logical element.
- 13. The method of claim 12, comprising performing an analysis of a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.
- 14. The method of claim 12, comprising identifying a domino element.
- 15. The method of claim 12, comprising identifying a bus retainer.
- 16. The method of claim 12, comprising identifying a latch.
- 17. The method of claim 12, comprising identifying a self-reset loop.
- 18. The method of claim 12, comprising identifying a combinatorial element.
- 19. An apparatus comprising:
 - a processor to find a loop in a circuit design, functionally analyze the loop, and extract a logical element in relation to the analysis result.
- 20. The apparatus of claim 19, wherein the processor is to perform a Depth First Search linear traversal.
- 21. The apparatus of claim 19, wherein the processor is to identify a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

- 22. The apparatus of claim 21, wherein the processor is to generate overall zero-delay collapsed functionality on an output of said group.
- 23. The apparatus of claim 21, wherein the processor is to identify a functional part that forms said group.
- 24. The apparatus of claim 21, wherein the processor is to determine a driving logic of said group.
- 25. The apparatus of claim 21, wherein the processor is to determine a driving control of said group.
- 26. The apparatus of claim 21, wherein the processor is to determine a stage feedback logic of said group.
- 27. The apparatus of claim 21, wherein the processor is to determine a stage feedback control of said group.
- 28. The apparatus of claim 21, wherein the processor is to determine a stage feedback type of said group.
- 29. The apparatus of claim 21, wherein the processor is to determine an asynchronous set and reset logics of said group.
- 30. The apparatus of claim 19, wherein the processor is to extract a logical element.
- 31. The apparatus of claim 30, wherein the processor is to perform an analysis of a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.
- 32. The apparatus of claim 30, wherein the processor is to identify a domino element.

- 33. The apparatus of claim 30, wherein the processor is to identify a bus retainer.
- 34. The apparatus of claim 30, wherein the processor is to identify a latch.
- 35. The apparatus of claim 30, wherein the processor is to identify a self-reset loop.
- 36. The apparatus of claim 30, wherein the processor is to identify a combinatorial element.
- 37. An apparatus comprising:
 - a dynamic random access memory; and
 - a processor to find a loop in a circuit design, functionally analyze the loop, and extract a logical element in relation to the analysis result.
- 38. The apparatus of claim 37, wherein the processor is to identify a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.
- 39. The apparatus of claim 38, wherein the processor is to identify a functional part that forms said group.
- 40. A machine-readable medium having stored thereon a set of instructions that, if executed by a machine, cause the machine to perform a method comprising:
 finding a loop in a circuit design;
 functionally analyzing the loop; and
 extracting a logical element in relation to the analysis result.
- 41. The machine-readable medium of claim 40, wherein the instructions result in identifying a group of at least one Channel Connected Sub-Network that forms at least one combinational loop and corresponds to a functional device.

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42. The machine-readable medium of claim 41, wherein the instructions result in identifying a functional part that forms said group.